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PATENT APPLICATION Exemplos Chiles Do. No. 1482-129

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Barrie Gilbert

Serial No.:

09/675,902

Examiner: Tung X. Nguyen

Filed:

September 28, 2000

Group Art Unit: 2829

For:

GAIN AND PHASE DETECTOR HAVING DUAL LOGARITHM HEREBY CERTIFY THAT THIS AMPLIFIERS

**AMPLIFIERS** 

Date:

August 7\_, 2002

Box Non-Fee Amendment Commissioner of Patents and Trademarks Washington, DC 20231

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## SUPPLEMENTAL RESPONSE TO OFFICE ACTION

Responsive to the Office Action dated March 5, 2002 and supplementing the Response to Office Action filed August 5, 2002, applicant submits the following.

## In The Specification

Replace the paragraph beginning at page 3, line 3 and ending at page 3, line 9 with the following paragraph:



"Log amp 10 will be referred to as part of channel A, which receives the input signal  $V_A$  and generates the logarithmic output signal  $V_{OUT\_A}$ . Likewise, log amp 12 will be referred to as part of channel B, which receives the input signal V<sub>B</sub> and generates the logarithmic output signal V<sub>OUT\_B</sub>. For purposes of illustration, the signals utilized in Fig. 4 are shown as single-sided voltages, but the present invention can be realized with differential voltage signals, differential or single-sided current mode signals, or any convenient combination thereof. The logarithmic output signals V<sub>OUT</sub> A and V<sub>OUT</sub> B are given by the following equations:"